CLAIMS

What is claimed is:

1. An integrated circuit comprising:

a control circuit to generate a first control signal according to a phase relationship between an input signal and a first clock signal;

a select circuit coupled to receive the first control signal from the control circuit and coupled to receive a second control signal, the select circuit being responsive to a select signal to select either the first control signal or the second control signal to be output as a selected control signal; and

a phase adjust circuit coupled to receive the selected control signal from the select circuit, the phase adjust circuit being responsive to the selected control signal to adjust the phase of the first clock signal.

2. The integrated circuit of claim 1 further comprising a receive circuit to sample the input signal in response to the first clock signal.

3. The integrated circuit of claim 1 wherein the phase adjust circuit includes circuitry to output a plurality of clock signals including the first clock signal, and wherein the control circuit comprises:

a receive circuit to capture a plurality of samples of the input signal in response to transitions of the plurality of clock signals; and

a phase control circuit to determine, based on the plurality of samples of the input signal, whether a transition of the input signal occurs before or after a transition of the first clock signal.

4. The integrated circuit of claim 3 wherein the first control signal is a digital signal having one of at least two possible states, and wherein the phase control signal includes circuitry to output the first control signal in either a first state or a second state of the at least two possible states based, at least in part, on whether the transition of the input signal occurs before or after the transition of the first clock signal.

5. The integrated circuit of claim 1 wherein the first control signal includes a first component signal that is asserted if the first clock signal lags the input signal and a second component signal that is asserted if the first clock signal leads the input signal.

6. The integrated circuit of claim 1 wherein the first control signal is an analog signal having a voltage level indicative of the phase relationship between the input signal and the first clock signal.

7. The integrated circuit of claim 1 wherein the first control signal is an analog signal having a current level indicative of the phase relationship between the input signal and the first clock signal.

8. The integrated circuit of claim 1 further comprising an input to receive the select signal from an external device.

9. The integrated circuit of claim 1 further comprising a programmable register to store a mode value, the select signal having either a first state or a second state according to the mode value, and the select circuit including circuitry to select the first control signal if the select signal is in the first state and to select the second control signal if the select signal is

in the second state.

10. The integrated circuit of claim 1 wherein the select circuit comprises a multiplexer circuit.

11. A method of operation within an integrated circuit, the method comprising:

determining a phase relationship between an input signal and a first clock signal;

generating a first control signal according to a phase relationship between an input signal and a first clock signal;

selecting either the first control signal or a second control signal to be output to a phase adjust circuit as a selected control signal; and

adjusting, in the phase adjust circuit, the phase of the first clock signal according to the selected control signal.

12. The method of claim 11 further comprising sampling the input signal in response to the first clock signal.

13. The method of claim 11 further comprising:

outputting a plurality of clock signals, including the first clock signal;

capturing a plurality of samples of the input signal in response to transitions of the plurality of clock signals; and

determining the phase relationship between the input signal and the first clock signal, at least in part, by determining, based on the plurality of samples of the input signal, whether a transition of the input signal occurs before or after a transition of the first clock signal.

14. The method of claim 13 wherein generating the first control signal comprises generating a

digital control signal having one of at least two possible states based, at least in part, on whether the transition of the input signal occurs before or after the transition of the first clock signal.

15. The method of claim 11 wherein generating the first control signal comprises generating a digital signal having a first and second component signals, the first component signal being asserted if the first clock signal lags the input signal and the second component signal being asserted if the first clock signal leads the input signal.

16. The method of claim 11 further comprising receiving the select signal from a device that is external to the integrated circuit.

17. The method of claim 11 further comprising storing a mode value in a programmable register within the integrated circuit, and wherein generating the select signal comprises generating the select signal according to the mode value.

18. The method of claim 11 further comprising

receiving a command to store a mode value; and

storing the mode value in a register within the integrated circuit; and

wherein generating the select signal comprises generating the select signal according to the mode value.

19. An integrated circuit device comprising:

a first clock data recovery (CDR) circuit to recover clock and data signals from a first signal line, the first CDR circuit including:

a first phase control circuit to generate a first control signal, and

a first phase adjust circuit to adjust the phase of a first recovered clock signal in response to the first control signal; and

a second CDR circuit to recover clock and data signals from a second signal line, the second CDR circuit including:

a second phase control circuit to generate a second control signal,

a select circuit coupled to receive the first and second control signals and being responsive to a select signal to select either the first control signal or the second control signal to be output as a selected control signal, and

a second phase adjust circuit to adjust the phase of a second recovered clock signal in response to the selected control signal.

20. The integrated circuit of claim 19 wherein the select circuit comprises a multiplexer circuit having a control input coupled to receive the select signal and having respective input ports coupled to receive the first and second phase signals from the first and second phase control circuits.

21. The integrated circuit of claim 19 further comprising additional CDR circuits each having a respective phase control circuit, select circuit and phase adjust circuit, the select circuit of each of the additional CDR circuits being responsive to a control input to output, as a selected control signal, either the first phase control signal or a phase control signal output by the phase control circuit of the additional CDR circuit, the phase adjust circuit of each of the additional CDR circuits being responsive to the selected control signal output by the select circuit for the additional CDR circuit to adjust the phase of a respective recovered clock signal.

22. The integrated circuit of claim 19 wherein the first CDR circuit further includes a first receive circuit to sample an input signal on the first signal line in response to the first recovered clock signal, and the second CDR circuit further includes a second receive circuit to sample an input signal on the second signal line in response to the second recovered clock signal.

23. The integrated circuit of claim 19 further comprising an input to receive the select signal from an external device.

24. The integrated circuit of claim 19 further comprising a programmable register to store a mode value, the select signal having either a first state or a second state according to the mode value, and the select circuit including circuitry to select the first control signal if the select signal is in the first state and to select the second control signal if the select signal is in the second state.

25. The integrated circuit of claim 19 wherein the second phase control circuit is responsive to the select signal to disable generation of the first control signal when the select signal indicates that the select circuit is to select the second control signal to be output as the selected control signal.

26. A method of controlling an integrated circuit, the method comprising:

outputting a first command to the integrated circuit to set a first clock data recovery (CDR) circuit within the integrated circuit to a first mode, the first CDR circuit including a select circuit to select a first control signal to adjust the phase of a first clock signal when the first CDR circuit is in the first mode;

delaying for a first time interval; and

outputting, after the first time interval, a second command to the integrated circuit to set the first CDR circuit to a second mode, the select circuit of the first CDR circuit being adapted to select a second control signal when the first CDR circuit is in the second mode, the second control signal being generated by a second CDR circuit.

27. The method of claim 26 wherein delaying for a first time interval comprises delaying until a predetermined number of cycles of a clock signal have transpired.

28. The method of claim 26 wherein outputting a first command to the integrated circuit to set the first CDR circuit to a first mode comprises outputting a command to the integrated circuit to store a mode value in a programmable register within the integrated circuit, the mode value indicating the first mode.

29. The method of claim 26 wherein outputting a first command to the integrated circuit to set the first CDR circuit to a first mode comprises outputting a mode signal to the integrated circuit, the mode signal being input to a select input of the select circuit to select the first control signal.

30. The method of claim 26 further comprising periodically repeating said outputting the first command to the integrated circuit, delaying for the first time interval, and outputting the second command to the integrated circuit.

31. The method of claim 26 further comprising:

detecting a predetermined condition; and

in response to detecting the predetermined condition, repeating said outputting the first

command to the integrated circuit, delaying for the first time interval, and outputting the second command to the integrated circuit.

32. The method of claim 31 wherein detecting a predetermined condition comprises detecting a change in temperature.

33. The method of claim 31 wherein detecting a predetermined condition comprises detecting a change in voltage.

34. The method of claim 31 wherein detecting a predetermined condition comprises detecting a loss of synchronization between the first clock signal and a data signal received in the first CDR signal.

35. A system comprising:

a first signal line;

a receive device coupled to the first signal line, the receive device having a first clock data recovery (CDR) circuit to recover clock and data signals from the first signal line, the first CDR circuit including control circuit, a select circuit and a phase adjust circuit, the control circuit being adapted to generate a first control signal according to a phase relationship between an input signal on the first signal line and a first clock signal, the select circuit being responsive to a mode value to select either the first control signal or a second control signal to be output as a selected control signal, the phase adjust circuit being adapted to adjust the phase of the first clock signal according to the selected control signal; and

a control device coupled to the receive device to provide the mode value thereto.

36. The system of claim 35 wherein the control device is coupled to provide the mode value to the receive device via the first signal line.

37. The system of claim 35 further comprising at least one additional signal line, the at least one additional signal line being coupled to the receive device and to the control device, the control device being adapted to provide the mode value to the receive device via the at least one additional signal line.

38. The system of claim 35 wherein the control device is adapted to output a first mode value to the receive device and then, after a first time interval, to output a second mode value to the receive device, the select circuit being responsive to the first mode value to select the first control signal to be output as the selected control signal, the select circuit being responsive to the second mode value to select the second control signal to be output as the selected control value.

39. The system of claim 38 further comprising a second signal line coupled to the receive device, and wherein the receive device includes a second CDR circuit to recover clock and data signals from the second signal line, the second CDR circuit including a control circuit to generate the second control signal according to a phase relationship between an input signal on the second signal line and a second clock signal.

40. The system of claim 35 wherein the receive device is implemented in a first integrated circuit and the control device is implemented in a second integrated circuit.

41. The system of claim 40 wherein the first and second integrated circuits are packaged in

separate integrated circuit packages.

42. The system of claim 40 wherein the first and second integrated circuits are packaged in the same integrated circuit package.

43. The system of claim 35 wherein the receive circuit and the control circuit are implemented within a single integrated circuit.

44. A method of testing an integrated circuit (IC) that includes a clock data recovery (CDR) circuit and a phase control port, the method comprising:

outputting a first command to the IC to set the CDR circuit to a first mode, the CDR circuit having a select circuit that responds to the first mode by selecting the phase control port to source a control signal instead of phase control circuit within the CDR circuit, the control signal being used by a phase adjust circuit within the CDR circuit to adjust the phase of a first clock signal; and

outputting a phase control signal to the phase control port of the integrated circuit device to adjust the phase of the first clock signal.

45. The method of claim 44 wherein outputting a first command to the integrated circuit to set the CDR circuit to a first mode comprises outputting a command to the integrated circuit to store a mode value in a programmable register within the integrated circuit, the mode value indicating the first mode.

46. The method of claim 44 wherein outputting a first command to the integrated circuit to set the first CDR circuit to a first mode comprises outputting a mode signal to the integrated circuit, the mode signal being input to a select input of the select circuit to select the phase

control port to source the control signal.

47. A method of testing an integrated circuit (IC) that includes a clock data recovery (CDR) circuit and a phase control port, the method comprising:

a. outputting a first command to the IC to set the CDR circuit to a first mode, the CDR circuit having a select circuit that responds to the first mode by selecting the phase control port to source a control signal instead of a phase control circuit within the CDR circuit, the control signal being used by a phase adjust circuit within the CDR circuit to adjust the phase of a first clock signal;

b. asserting a phase control signal at the phase control port of the integrated circuit device for a first predetermined time interval, the phase adjust circuit within the CDR circuit being responsive to the phase control signal to adjust the phase of the first clock signal;

c. deasserting the phase control signal for a second predetermined time interval; and

d. measuring the first clock signal with a signal measuring device while repeating actions b and c at least until the phase of the first clock signal has progressed through a predetermined portion of a cycle of the first clock cycle.

48. The method of claim 47 wherein the predetermined portion of a cycle of the first clock cycle is an entire cycle of the first clock cycle.

49. The method of claim 47 wherein the phase adjust circuit responds to assertion of the first control signal by advancing the phase of the first clock signal.

50. The method of claim 47 wherein the first predetermined time interval is selected to allow

the phase adjust circuit to advance the phase of the first clock signal by a predetermined phase angle.

51. The method of claim 47 wherein measuring the first clock signal with a signal measuring device comprises measuring the first clock signal with an oscilloscope.

52. An integrated circuit device comprising:

a first signal generator to generate a first test signal;

a receive circuit having an input switchably coupled to receive the first test signal from the first signal generator, the receive circuit including circuitry responsive to a first clock signal to capture samples of the first test signal;

a clock data recovery (CDR) circuit having a control circuit, a select circuit and a phase adjust circuit, the control circuit being adapted to generate a first control signal based on the samples of the first test signal, the select circuit being responsive to a select signal to select either the first control signal or a second control signal to be output as a selected control signal, and the phase adjust circuit being responsive to the selected control signal to adjust the phase of the first clock signal; and

a compare circuit to compare the samples of the first test signal to a compare signal.

53. The integrated circuit device of claim 52 wherein the first signal generator is a linear feedback shift register and the first test signal is a pseudo random bit sequence.

54. The integrated circuit device of claim 52 further comprising a transmit circuit having an input and an output, the input of the transmit circuit being switchably coupled to receive the first test signal from the first signal generator, and the output of the transmit circuit

being switchably coupled to the input of the receive circuit.

55. The integrated circuit device of claim 52 further comprising a mode control circuit to store a mode value indicative of an operating mode of the integrated circuit device, the mode control circuit outputting a test mode signal when the mode value is indicative of a test mode of operation, the test mode signal switching the input of the receive circuit to be coupled to receive the first test signal.

56. The integrated device of claim 52 wherein the compare circuit includes a second signal generator to generate the compare signal.

57. The integrated circuit device of claim 52 wherein the first signal generator and the second signal generator are designed to generate identical signals.

58. The integrated device of claim 52 wherein the first signal generator is coupled to provide the first test signal to the compare circuit, the compare signal being the first test signal.

59. A method of testing an integrated circuit that includes a clock data recovery (CDR) circuit and a phase control port, the method comprising:

a. setting the CDR circuit to a test mode in which a select circuit within the CDR circuit selects the phase control port to source a control signal instead of a phase control circuit within the CDR circuit, the control signal being used by a phase adjust circuit within the CDR circuit to adjust the phase of a first clock signal;

b. inputting a test signal to a receiver of the CDR circuit;

c. comparing the test signal against samples of the test signal generated by the CDR circuit;

d. asserting an error signal if the test signal does not match the samples;

e. asserting a phase control signal at the phase control input to adjust the phase of the first clock signal; and

f. repeating actions c through e to determine a maximum phase and minimum phase of the first clock signal for which the error signal is not asserted.